Memories of the Future: Operation and Manufacturing of Technology for the Next Decade

• Tom Coughlin, Coughlin Associates
• Ed Grochowski, Computer Storage Consultant
Outline

• The Promise of Non-Volatile Memory
• Non-Volatile Memory Technology
• MRAM Demand and Capital Equipment
• Conclusions
The Promise of Non-Volatile Memory
Memory/Storage Hierarchy

• Qualitative tradeoffs between volatile (and non-volatile) memory and non-volatile storage technology
  – costs to store data ($/TB)
  – performance of the storage technology (IOPS) or data rates).
Computer Memory Opportunities
(from SNIA Winter Symposium)

Significant hierarchy gap exists in current scale-out architectures

- QPI: 80ns
- L1 Cache: 1.5ns
- L2 Cache: 4ns
- L3 Cache: 15ns
- DDR3: 300ns
- SATA SSD: >1M ns
- PCIX: 9,000ns
- SAS HDD: 25M ns
Progression of Storage Technologies with Non-Volatile Solid State Storage

(Presentation by Tony Roug of Intel at a SNIA SSSI meeting in January 2013)
NVDIMM Activities

- NVDIMM Activity (image from SNIA Winter Symposium)
- Shows NVDIMM Controller with Ultracapacitors to complete writes if power is lost
- SNIA NVDIMM Working Group
Implications of Persistent Memory

• NV memory retains its data even when power off—thus instant recovery of state before power down is now possible
• NV memory with the right SW changes can provide much better latencies than current systems and SW
• Non-volatile memory will save power since refreshes not needed
• Persistent memory creates new opportunities to share that memory between different computers or computer chips using Remote Direct Memory Access (RDMA)
• Embedded NVM technology can lead to “logic-in-memory architecture” for future SoC—this can lead to new distributed computer architectures
Storage Latency Storage Latency with Current and Future NV Solid State NV Technologies
(from NVMP talk at SNIA Winter Symposium.)

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Science Fiction Into Reality

• Enable new industries and applications.
  – The development of an Internet of Things (IoT) that will make social networking extend to the things we own,
  – Improved network connectivity and data transfers,
  – Accelerate the development of self-driving cars,
  – Help users with disabilities be self-reliant,
  – Provide the technology to capture and store life logs,
  – Create an immersive artificial reality,
  – Popularize mobile device tricorders, and
  – Create a host of things that have been the subjects of Science Fiction, and even things we haven’t dreamed of yet.
Challenges Of Persistent Memory

• If the memory isn’t cleared by rebooting a system, then reboots to recover functionality with corrupted data won’t work
• There will need to be a special reboot and clear function that erases and recovers data in memory
• Or, and this may be an even better solution, we need to built devices and software that are self-monitoring and self correcting so we don’t need to reboot in order to retain functionality
Non-Volatile Memory Technologies
Comparison of Solid-State Memory Technologies (1)

<table>
<thead>
<tr>
<th></th>
<th>SRAM</th>
<th>DRAM</th>
<th>NOR Flash</th>
<th>NAND MLC Flash</th>
</tr>
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<tbody>
<tr>
<td>Non-volatile</td>
<td>N</td>
<td>N</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Memory cell factor ($F^2$)</td>
<td>50-120</td>
<td>6-10</td>
<td>10</td>
<td>4-5</td>
</tr>
<tr>
<td>Read time (ns)</td>
<td>1-100</td>
<td>30</td>
<td>10</td>
<td>50</td>
</tr>
<tr>
<td>Write/erase time (ns)</td>
<td>1-100</td>
<td>50</td>
<td>$10^5/10^7$</td>
<td>$10^6/10^5$</td>
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<tr>
<td>Number of rewrites</td>
<td>$10^{16}$</td>
<td>$10^{16}$</td>
<td>$10^5$</td>
<td>$10^3$</td>
</tr>
<tr>
<td>Power consumption at write</td>
<td>Low</td>
<td>Low</td>
<td>High</td>
<td>Med</td>
</tr>
<tr>
<td>Required input voltage (V)</td>
<td>None</td>
<td>2</td>
<td>6-8</td>
<td>1.8</td>
</tr>
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</table>
## Comparison of Solid-State Memory Technologies (2)

<table>
<thead>
<tr>
<th></th>
<th>FeRAM</th>
<th>RRAM</th>
<th>Magnetic field write MRAM</th>
<th>PRAM</th>
<th>STT MRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Non-volatile</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Memory cell factor ($F^2$)</td>
<td>16-32</td>
<td>4-6</td>
<td>16-32</td>
<td>5-8</td>
<td>5-7</td>
</tr>
<tr>
<td>Read time (ns)</td>
<td>20-50</td>
<td>10-20</td>
<td>3-20</td>
<td>5-20</td>
<td>3-15</td>
</tr>
<tr>
<td>Write/erase time (ns)</td>
<td>50</td>
<td>20</td>
<td>10-20</td>
<td>&gt;30</td>
<td>3-15</td>
</tr>
<tr>
<td>Number of rewrites</td>
<td>$10^{12}$</td>
<td>$10^5$</td>
<td>$10^{15}$ min</td>
<td>$10^{12}$</td>
<td>$10^{15}$ min</td>
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<tr>
<td>Power consumption at write</td>
<td>Low</td>
<td>Low</td>
<td>Somewhat high</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Required input voltage (V)</td>
<td>2-3</td>
<td>1.2</td>
<td>3</td>
<td>1.5-3</td>
<td>1.5</td>
</tr>
</tbody>
</table>

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Performance and Density Roadmap for Memory and Storage Technologies

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NAND Flash Memory Circuit Density Roadmap

Production Year

Circuit Capacity Mbits

1000000
100000
10000
1000
100
10

Floating Gate

Advanced Technology

Charge Trap

SLC

MLC

3-D

1 Gb 130 nm

2 Gb 90 nm

8 Gb 65 nm

4 Gb 90 nm

1 Gb 130 nm

512 Mb 180 nm

256 Mb 250 nm

64 Mb 250 nm

32 Mb 400 nm

16 Mb 600 nm

>256 Gb 19 nm

256 Gb 12 nm

128 Gb 19 nm

80 Gb 24 nm

64 Gb 24 nm

16 Gb 45 nm

512 Mb 180 nm

256 Mb 250 nm

64 Gb 250 nm

32 Mb 400 nm

16 Mb 600 nm

Ed Grochowski

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Chip Capacity Projections for Various Memory Technologies

Projected Capacity Increase/Chip

Ed Grochowski
based on T. Liu ISSCC2013

PCRAM

MRAM

NAND Flash

STTMRAM

ReRAM

Storage Capacity Mb sights

Production Year

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3D Memories

3D Flash Memory Cells, Toshiba VLSIT 2009

3D Vertical RRAM, Source: Chen IEDM 2012

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ReRAM or RRAM Cross Point Array

- This technology perhaps shows the most promise as a NAND Flash replacement
- The most promising RRAM structures involve multi-film diodes using compatible materials as an integral part of the unit cell to eliminate the requirement for a larger CMOS device

From 2013 Flash Memory Summit
Ferroelectric RAM (FeRAM)

- This family of devices consists of a CMOS transistor and a variable capacitor, and therefore is a 1T/1C type NV storage cell.
- FeRAM devices exhibit remarkable insensitivity to radiation, compared with FLASH and DRAM so that these NV storage devices are in demand for military applications.
Phase Change Memory (PCRAM)

- PCRAM cells are bit addressable, are true NVRAM’s, and yield high-density arrays.
- The phase change is accompanied by a resistance change, i.e. the crystalline phase has low resistance and the amorphous phase has higher resistance.
Magnetic Race Track

- The MRT employs the motion of domains through a vertically oriented magnetic material such as a permalloy wire (a NiFe alloy)
- By connecting a series of MRT nano-wires, a type of magnetic shift register may be configured.
- A single read and write head positioned at one location of the column determines the polarity of these domains records them accordingly.

Magnetic Race Track Memory Configured as Shift Register (Stuart Parkin, IBM)
Other Memory Technologies

- Carbon Nanotubes
- Polymeric Ferroelectric RAM (PFRAM)
- Ferroelectric Field Effect Transistor RAM (FeFET RAM)
Magnetic RAM (MRAM)

- Three Major MRAM memory architectures
  - Toggle Mode (field driven)
  - Spin Torque Transfer (STT)
  - Magnetothermal MRAM (Heat Assisted)

STT MRAM Stack on Single CMOS Transistor
Spin Momentum Transfer

- STT MRAM uses the electron spin to create a memory element

<table>
<thead>
<tr>
<th></th>
<th>STT MRAM</th>
<th>DRAM</th>
<th>SRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read Time (ns)</td>
<td>3-</td>
<td>30</td>
<td>1-100</td>
</tr>
<tr>
<td>Write Time (ns)</td>
<td>3-15</td>
<td>50</td>
<td>1-100</td>
</tr>
<tr>
<td># Rewrites</td>
<td>$&gt;10^{15}$</td>
<td>$10^{16}$</td>
<td>$10^{16}$</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>1.5</td>
<td>2</td>
<td>None</td>
</tr>
</tbody>
</table>

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Possible STT MRAM Device Cell Architectures

MRAM (DRAM Replacement) Memory/Storage Cell

SRAM Replacement (High Performance Memory)
Comparison of DRAM and STT MRAM

- STT MRAM Replaces DRAM capacitive element with a resistive element
- STT MRAM performance is close to DRAM and near SRAM
- STT MRAM is Non-volatile, DRAM requires refresh
Future STT MRAM Replacement for SRAM

6T SRAM (Memory Cell)

Write Current

Read Current

STT RAM (Performance Memory)
Estimated STT MRAM DRAM and SRAM Replacement

Read Latency (s)

Relative Cell Area ($F^2$)

STT MRAM single transistor

STT SRAM multi transistor
Everspin 64 Mbit STT MRAM Chip Used for Caching
MRAM Demand and Capital Investment
$/GB for Memory Technologies

(includes data from Jim Handy, Objective Analysis)
Annual Memory Capacity Shipments

(includes data from Jim Handy, Objective Analysis)
MRAM Manufacturing Process Flow

- First comes CMOS transistor production after which the MRAM layers must be deposited using a physical vapor deposition technology.
- After depositing this stack the basic pattern, MRAM Manufacturing Process Flow must be defined on the surface of the MRAM stack.
- This pattern is then used to control etching of the MRAM device.
- Following the construction of MRAM devices connected to their CMOS transistors the devices go through testing and mapping out the bad memory cells.
Equipment for MRAM Production

Singulus Timaris PVD Cluster Tool Platform

Canon I-Line Stepper

ISI WLA 3000 Quasi-Static Tester

Veeco Nexus Ion Beam System

Tokyo Electron Magnetic Annealing Tool

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Revenue Estimates for MRAM Equipment

![Graph showing equipment spending (in $M) from 2013 to 2019 for different categories: Test & Other Equipment, Ion Etch Equipment, Patterning Equipment, and PVD Equipment. The graph indicates an increasing trend in spending over the years.]
Conclusions

• Many Candidates for NV memory/storage – RRAM, STT MRAM, PRAM, FRAM, each with specific trade-offs
• Advantages: Power Savings, Scalability, Density
• Architectural System Evolution—new applications, use spin versus current
• RRAM replacement for flash after 2020
• STT-MRAM, RRAM Replacement for SRAM and DRAM
• STT-MRAM Very Compatible With current CMOS Processing
• MRAM Production drives capital investment